REMARKS

In the Office Action dated January 26, 2005, claim 1, 2, 4, 5, 9, and 37 were rejected under 35 U.S.C. § 103 over U.S. Patent No. 5,678,026 (Vartti) in view of U.S. Patent No. 5,740,401 (Hanawa); claims 10-12, 14-17, and 38-42 were rejected under § 103 over Vartti in view of Hanawa and U.S. Patent No. 6,105,094 (Lindeman); claim 3 was rejected under § 103 over Vartti in view of Hanawa, and U.S. Patent No. 6,092,156 (Schibinger); and claim 13 was rejected under § 103 over Vartti in view of Hanawa, Lindeman, and Schibinger.

Applicant acknowledges the allowance of claims 22-36, and the indication that claims 6-8, 18, and 19 contain allowable subject matter. Claim 6 has been amended from dependent form to independent form, with its scope *unchanged*, to place the claim in condition for allowance. The only changes made to claim 6 are to form, with the term "first" added before "memory location" at line 26, and "first memory locations" changed to "first memory location" at line 29-30.

Claims 1, 2, 4, and 5 have been cancelled, without prejudice, to render the rejections of the claims moot.

Each of independent claims 10 and 41 were rejected as being obvious over Vartti, Hanawa, and Lindeman. The obviousness rejection of claim 41 is addressed first. It is respectfully submitted that a *prima facie* case of obviousness has not been established with respect to claim 41 for at least the following two reasons: (1) the hypothetical combination of Vartti, Hanawa, and Lindeman does not teach or suggest *all* elements of the claim; and (2) no motivation or suggestion existed to combine the teachings of Vartti, Hanawa, and Lindeman to achieve the claimed invention. *See* M.P.E.P. § 2143 (8th ed., Rev. 2), at 2100-129.

With respect to claim 41, the Office Action stated that "the limitations of the claim are rejected as the same reasons as set forth in claim 10." 1/26/2005 Office Action at 7. In the rejection of claim 10, the Office Action conceded that neither Vartti nor Hanawa "specifically teaches communicating between the multiprocessor node through a switch and sending access request information associated with the exclusive access or shared memory of the first multiprocessor node to the second multiprocessor node by the switch." *Id.* at 5-6. The Office Action relied upon Lindeman as teaching "a method for allocating exclusive shared resource in a computer system comprising an access arbiter unit functioning as a switch communicating

between multiprocessor node [sic] in order to guarantee the bandwidth of data transfer (col. 7 lines 9-61)." *Id.* at 6.

It is noted that the subject matter of claim 41 is not the same as the subject matter of claim 10; thus, the rejection of claim 41 based on the rejection of claim 10 is improper. Specifically, claim 41 recites a switch coupled to the multiprocessor nodes, where the switch is to receive access request information and to send the access request information to the multiprocessor *nodes* (note plural sense of "multiprocessors nodes") for storage of the access request information in the respective registers of the memory controllers.

Thus, even if the arbiter unit of Lindeman can be considered a switch according to claim 41, it is noted that the arbiter unit of Lindeman does not send access request information (associated with an exclusive access) to multiprocessor *nodes*. The stated function of the arbiter unit in Lindeman is to prevent a data storage host controller 220 (see Fig. 3 of Lindeman) from gaining exclusive access to a computer main memory unit 206 by way of the system primary bus 202 during a time that a digital video host controller 228 is transferring data from the computer main memory unit 206 in an isochronous data transfer mode. Lindeman, 7:11-21. There is no indication or any suggestion of the arbiter unit of Lindeman sending access request information (associated with an exclusive access) to plural multiprocessor nodes. As conceded by the Office Action, neither Vartti nor Hanawa teaches a switch according to claim 41. Therefore, the hypothetical combination of Vartti, Hanawa, and Lindeman fails to teach or suggestion all elements of claim 41, and more specifically, the hypothetical combination of the references fails to teach or suggest a switch to send access request information associated with an exclusive access to plural multiprocessor nodes for storage of the access request information in the respective registers of the memory controllers of the multiprocessor nodes. For at least this reason, the *prima facie* case of obviousness fails.

Moreover, there simply did not exist any motivation or suggestion to incorporate the arbiter unit of Lindeman into the systems of Vartti or Hanawa. The Lindeman system describes an arbiter unit in a typical single-processor environment, which includes a host processor 204, a primary PCI bus 202, and a secondary PCI bus 214 (see Fig. 2 of Lindeman). The primary PCI bus 202 and secondary PCI bus 214 are connected to various peripheral devices, such as a graphics hardware card 258, a data storage host controller 220, and a digital video data host

controller 228. The arbiter unit described in Lindeman is part of a bus request controller unit 234 that is coupled to the data storage host controller 220 and digital video data host controller 238. Lindeman, 5:66-6:2. The bus request controller unit 234 arbitrates for access to the main memory unit 206. Lindeman, 6:39-62.

There is no suggestion by Lindeman that its bus request controller unit or arbiter unit can be used with multiprocessor nodes. Nor is there any suggestion in either Vartti or Hanawa of any desirability to use an arbiter unit similar to the Lindeman arbiter unit in the Vartti or Hanawa system. The arbiter unit of Lindeman arbitrates between requests from a data storage host controller 220 and digital video data host controller 228, which are peripheral devices connected to a secondary bus 214. Vartti and Hanawa propose completely different solutions for handling requests from multiple processors in a multiprocessing system – therefore, since there was no suggestion of any desirability to incorporate the teachings of Lindeman into the Vartti or Hanawa systems, it is respectfully submitted that no motivation or suggestion existed to combine the teachings of Vartti, Hanawa, and Lindeman to achieve the claimed invention. A *prima facie* case of obviousness has not been established with respect to claim 41 for at least this additional reason.

Withdrawal of the obviousness rejection of claim 41 is respectfully requested.

A *prima facie* case of obviousness has also not been established with respect to claim 10 for at least the reason that no motivation or suggestion existed to combine the teachings of Vartti, Hanawa, and Lindeman to achieve the claimed invention, as discussed above with respect to claim 41.

Dependent claims are allowable for at least the same reasons as corresponding independent claims.

Moreover, with respect to dependent claim 40, which depends indirectly from claim 10, the asserted combination of Vartti, Hanawa, and Lindeman also fails to disclose or suggest storing access request information associated with an exclusive access in a register in the switch, where the access information in the first register of the first memory controller and in the second register of the second memory controller are *shadow copies of the access request information in the register of the switch*. There is absolutely no suggestion anywhere in Vartti, Hanawa, or Lindeman of this feature of claim 40, where access request information is stored in the register in

the switch, and where the access information in registers of first and second memory controllers are shadow copies of the access request information in the switch register. The obviousness rejection of claim 40 is defective for this additional reason.

Claim 42, which depends from claim 41, is additionally allowable for reasons similar to those of claim 40.

Allowance of all claims is respectfully requested. The Commissioner is authorized to charge any additional fees and/or credit any overpayment to Deposit Account No. 08-2025 (200301872-1).

Respectfully submitted,

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